REMARKS

Claims 1-16 are pending. Claims 6-11 have been withdrawn. By this Response, claims 1, 12 and 13 are amended and claims 14-16 added. Reconsideration and allowance based on the above amendments and following remarks are respectfully requested.

The Office Action rejects claims 1 and 13 under 35 U.S.C. §103(a) as being unpatentable over Kuroda (US 5,487,029) in view of Clemons (US 4, 599,709); claims 2-5 under 35 U.S.C. §103(a) as being unpatentable over Kuroda, Clemons and Dierke (US 5,734,615) and claim 12 under 35 U.S.C. §103(a) as being unpatentable over Kuroda, Clemons and Seyyedy (US 5,969,380). These rejections are respectfully traversed.

For reasons of brevity, applicants remarks filed in the Response dated July 5, 2005 are hereby incorporated by reference.

Claims 1 and 12 have been amended to now recite, *inter alia*, where each memory cell is at all times in ohmic contact with a word line and a bit line. Claim 13 has been amended to recite, *inter alia*, where the memory material is at all times an ohmic contact with the first and second set of electrodes.

Claims 1 and 12 have also been amended to recite, *inter alia*, where each separate bit line assigned to a segment is connected with a different associated sensing means.

Applicants respectfully submit that neither Kuroda, Clemons, Dierke or Seyyedy alone or in combination teach or suggest the passive matrix memory which includes the above claimed limitations.

Applicants respectfully submit that there is a significant difference between active and passive memories which preclude them from teaching essential features of each other. In active

memories, the memory cells outside an addressing operation are disconnected from at least one of the addressing electrodes by a switch such as a transisor. Thus, either the source or drain of the transistor of the non-addressed memory cell must be disconnected from the addressing electrodes. Moreover, the electrodes then must be gated by an additional gate electrode line. This makes the active matrix addressable memory more complicated more power consuming and require much greater real estate.

In contrast, in passive memory devices, each of the memory locations are in continuous ohmic contact with the word and bit lines through the memory medium which create each of the memory cells. The use of a transistor or other switching device on the memory cell locations precludes those memory cells from being in continuous ohmic contact.

The essential features of these two types of memories are entirely unique to each of the different types of memories. As noted above, applicants have amended the independent claims to clarify this difference between a passive memory from the active memories taught by the applied references.

Specifically, applicants respectfully submit that Kuroda teaches an active matrix addressable ferroelectric memory cell which is switched into contact with one of the access electrodes, the word line or the bit line, for an addressing operation. Each memory cell comprises a switch, for instance a transistor that is activated via a separate electrode line for pulsing the gate of the transistor. Kuroda does not teach or suggest each memory cell being at all times in ohmic contact with a bit line and word line.

Clemons teaches an SRAM (static random access memory) which creates memory cells that do not need to be periodically refreshed. The SRAM of Clemons is a not a ferroelectric memory at all. As with Kuroda, Clemons requires access transistors that must be used in an

addressing operation. Thus, as with Kuroda, Clemons does not provide memory cells which are in continuous ohmic contact at all times.

Applicants respectfully submit that both Kuroda and Clemons teach memories which require transistors which for each memory cell is used in order to address the memory cell. These memories are in stark contrast to the passive memory device of applicant's present invention in which each memory cell is at all times in ohmic contact with a word line and a bit line that form the memory cell.

Further, Clemons teaches dividing a bit line into byte blocks such that, for example, four bit lines correspond to a single byte block and hence a byte can be stored in this block and read out to the I/O line to which there may be attached a sense amplifier. Clemon's system allows for a parallel readout of a byte by simple accessing all memory cells in a single byte block. Each bit line in a segment is not associated with a different sensing means.

Thus, applicants respectfully submit that Kuroda and Clemons fail to teach or suggest where each separate bit line assigned to a segment is connected with a different associated sensing means. In both Kuroda and Clemons, the bit lines in the alleged segments are grouped such that at least two or more of the bit lines in each group are associated with the same sensing device. Thus, applicants respectfully submit that Kuroda and Clemons fail to teach or suggest where each separate bit line assigned to a segment is connected with a different associated sensing means.

Furthermore, Dierke and Seyyedy fail to make up for the deficiencies of Clemons and Kuroda. Dierke is provided to teach aspects of the dependent claims and Seyyedy is provided to teach the use of a volumetric data storage apparatus with a plurality of stacked layers.

Applicants respectfully submit that neither Dierke nor Seyyedy teach or suggest the features argued above absent in the teachings of Kuroda and Clemons.

Therefore, in view of the above, applicants respectfully submit that Kuroda, Clemons, Dierke and Seyyedy and any combination fail to teach each and every feature of applicant's claims as required. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Further, regarding newly added dependent claims 14-16, applicants respectfully submit that neither the references teach or suggest providing the number of sensing means equal to the number of bit lines within each segment where each segment contains the same number of bit lines, such that each line in each segment is sensed at a different sensing means.

Conclusion

For at least the reasons above, it is respectfully submitted that claims 1-16 are distinguishable over the cited art. Favorable consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings (Reg. No. 48,917) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant respectfully petitions for a one (1) month extension of time for filing a reply in connection with the present application, and the required fee of $60.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: January 23, 2006

Respectfully submitted,

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